AMENDMENT TO THE SPECIFICATION

Please amend the specification as follows:

Please amend the fourth full paragraph on page 14 to read:

According to one embodiment of the present invention, rather than asserting its lock signal, a designated component will transmit (step S860) a lock indication signal to each component that is capable of accessing the address table 84. The lock indication signal may simply specify that the designated component is accessing the address table 84, or it may further specify which specific bin entry 96 within the address table 84 is currently being accessed by the designated component. Once the lock signal has been asserted, and/or the lock indication signal has been transmitted, the designated component will then access the address table 84 as indicated at step S870. The designated component will continue to access the address table 84 until it completes its transaction. During this time period, the other components will normally not be able to access the address table 84.

Please amend the third full paragraph on page 16 to read:

At step S950, the CPU interface 50 sets the acknowledge bit 212 to indicate that it has successfully locked the desired bin entry 96 for access by the CPU 32. At step S960, the CPU interface 50 asserts its lock signal to indicate that it has placed a lock on the address table 84 and/or a specific bin entry 96 stored therein. As previously indicated, the CPU interface 50 may further provide an indication of which specific bin entry 96 within the address table 84 it currently has a lock on. Depending on the specific embodiment of the present invention being implemented, the CPU interface 50 may further output (step S970) a lock indication signal to all components that are capable of accessing the address table 84. When the CPU 32 can access the address table 84, it will check to see if the CPU interface 50 has set the acknowledge bit 212.